A High Speed Low Power 10T SRAM with high Robustness

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Abstract— **In this paper, a High Speed Low Power 10TSRAM (HS10T) with good read stability and write ability is proposed. The proposed SRAM (Static Random Access Memory) circuit uses single-ended bit line paths for the read and write operations. HS10T has a strong cross coupled structure of standard inverter with stacked transistor and Schmitt-Trigger (ST) based inverter, which improves the speed of operations as well as low power consumption. The transistors are sized to optimize the delay, area and power consumption of the cell configuration. The performance of the proposed SRAM is verified using a 250nm Tanner EDA (Electronic Design Automation) tool with 2.5 volts as input. Compared to the similar 10TSRAM, the proposed HS10T cell has a higher noise margin, more speed and lower power consumption.**

Keywords—SRAM; HS10T; 10TSRAM; Tanner EDA; Schmitt-Trigger (ST)

I. INTRODUCTION

Since the invention of batteries and portable electronic equipment, studies are being conducted to reduce the power consumption. Similarly as technology advances, the size of devices shrinks and speed of the devices increases. The importance of speed and power consumption is indeed increased when it comes to medical devices like implantable pacemakers and defibrillators.

SRAM is an inevitable component in all electronic devices and has a major role in power consumption and performance. It occupies a significant portion of SoC (System-on-a-Chip) and is used most of the time for the operation of the device. The speed of the SRAM must be high to meet real time operations, and at the same time it must be a reliable and low power component for a long life. Different techniques are available to reduce power consumption. One method is the supply voltage scaling [1], [2]. But this method degrades the performance of the SRAM. Therefore, reducing the power while maintaining performance is a challenging task. Other methods to reduce the overall power consumption are by controlling the leakage current and standby power of the SRAM [3], [4].

II. RESERCH OF EXISTING MODELS OF SRAM CELL

Starting with conventional 6TSRAM cell, many models of SRAM cells are available, with each configuration addressing the different challenges. The main problem that we are facing in the conventional 6TSRAM cell is read stability due to unwanted transitions [5]. The solutions to stabilize the SRAM cell from these unwanted transitions are either by preventing the MOSFET from a false transition due to which state change happened in the opposite node or by preventing the opposite node from this false transition. In [6], a single-ended 7T SRAM cell is proposed by Takeda, where an additional MOSFET is used in the pull-down path of the inverter, which prevents the node of that inverter from the false transition of the opposite node during the read operation. In [7], Verma proposed a single-ended 8T SRAM cell that employs sense-amplifier redundancy. In this proposal, two additional transistors are added to the standard 6T SRAM, providing separate read and write paths. An 8T SRAM cell with enhanced write-read operation is proposed in [8] by Pasandi using write-assist technique. In this configuration, additional NMOS and PMOS transistors are added to the pull-down and pull-up path of the complement side inverter to achieve more write ability. In [9], Satish proposed a single ended 9T SRAM cell by adding one more transistor to the 8T SRAM cell [7]. This configuration provides separate read and write paths plus controlled read operation. A half-select bitline sharing 9T SRAM cell is proposed in [10] by Shin, where read stability is enhanced using a separate read path and it employs a differential write structure. In [11], Pal proposed a 9T SRAM

cell based on transmission gate to achieve high read stability and write ability. It utilized the write-assist technique and obtained low power consumption due to single-end bitline structure. A one-sided Schmitt-Trigger based 9T SRAM is proposed in [12] by Cho, which employs a cross coupled structure of standard and ST inverters. Reduced dynamic power and enhanced read stability are obtained by this structure. In [13], Kim proposed a single ended 10T SRAM cell. Similar to 8T SRAM cell [7], it has separate read and write paths with two additional transistors to reduce leakage during read operation. In [14], Jaydeep proposed a Schmitt-Trigger (ST) based single ended 10T SRAM cell [ST10T]. It has a built-in feedback mechanism that provides more tolerance for process variations. The ST10T cell read stability and write ability are better than the conventional 6TSRAM cell. In [15], Erfan proposed a Low Standby Power 10T SRAM (LP10T) cell with high read stability and write ability. It uses a cross-coupled structure between an inverter with stacked transistor and a Schmitt-Trigger-based inverter.

In this paper, a new configuration is proposed to enhance the performance of LP10T [15], and based on the simulation result, a comparison is carried out between LP10T and modified configuration cell.

A. Existing Low standby power 10TSRAM(LP10T)

TABLE I. LP10T CONTROL SIGNALS FOR DIFFERENT MODES

Signals	Operations			
	Hold	***Read***	***Write '0'***	***Write '1'***
RBL	1	1	1	1
WBL	1	1	0	1
RWL	0	1	0	0
WWL	0	0	1	1
WWLA	1	1	1	0

Fig.1 shows the existing Low Standby power 10T SRAM cell. It employs an inverter with stacked transistor (PUL, PDL1 and PDL2) at one storage node and a Schmitt trigger- based inverter (PUR, PDR2, PDR1 and NF) at the opposite node. It has a single-ended structure with separate bit lines for read and write operations. Transistors ACL1 and ACR1 are write access transistors in pass transistor logic. Both of them are controlled by the control signal write word line (WWL). Transistor ACL2 is a read-access transistor controlled by read word line (RWL) control signal. The transistor PDL2, which has role in assisting read and write operations is controlled by WWLA signal. The drain of the NF transistor in ST inverter and the drain of the write access transistor ACR1 are connected with WWLA. The ST inverter used in the right part of the cell is more robust due to its high trip voltage. Transistor NF provides negative feedback in the ST inverter, which weakens PDR2 and in effect the trip voltage increases at the input side of the ST. Due to this advantage, small transition at the counter part will not produce any unwanted state changes, especially in the case of read operation.

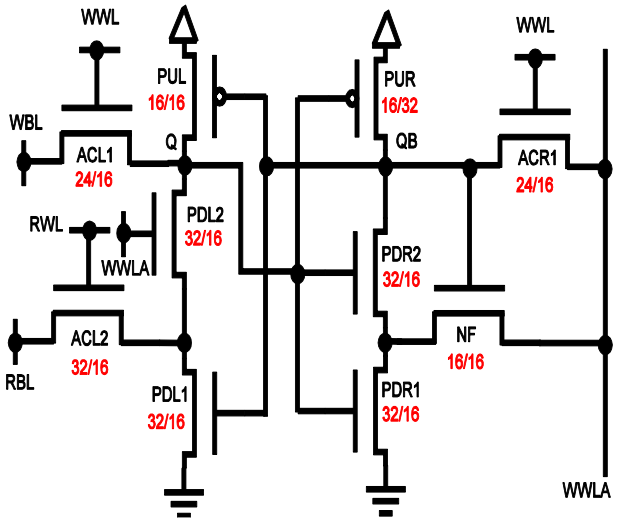

Fig. 1. Low Standby Power 10TSRAM(LP10T)

The control signals for different operations are shown in TABLE I. Sizing is done for all transistors to optimize the area, delay and power dissipation. In the case of ST inverter, due to its high trip voltage it is hard to change the output from '1' to '0'. Therefore, the length of the pull-up transistor (PUR) is doubled to equalize the margins of '0' and '1'.

The LP10T cell is simulated using tanner EDA tool in 250nm technology and obtained the results. Transient analysis done with T Spice commands to measure the delay for all the control signals. All the modes including Hold, Read and Write operations are verified from the simulation result. LP10T is built in 250nm technology, shown in Fig. 2

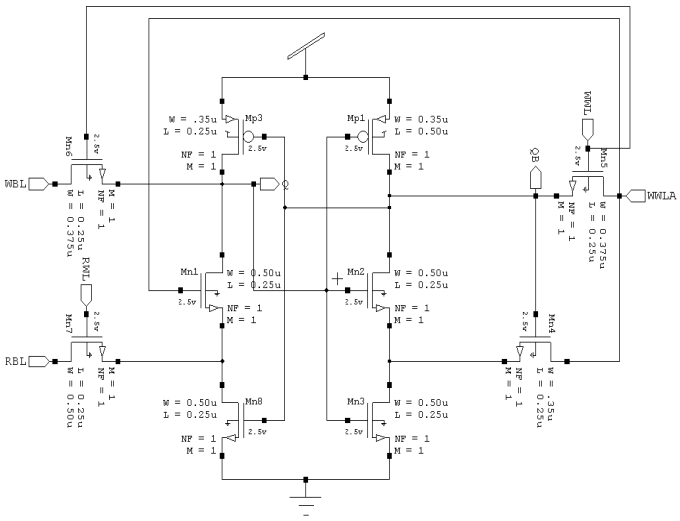

Fig. 2. LP10T cell build in Tanner EDA

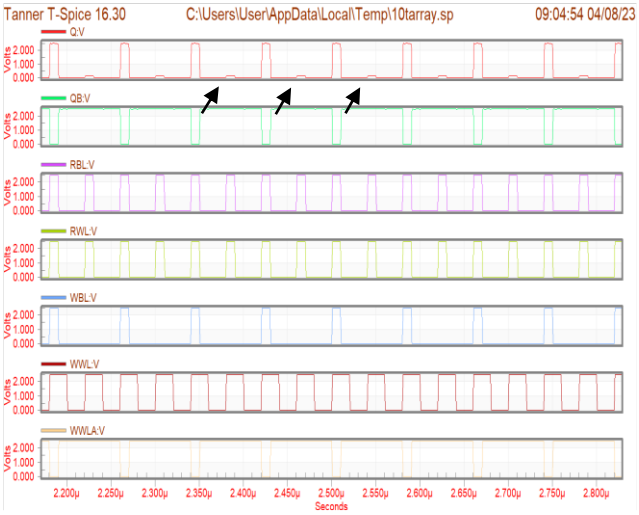

Fig. 3. Simulation result of LP10T

Fig. 3 shows the transient analysis result of LP10T. Read delay and Write delays are calculated for comparison purposes with the new proposed configuration cell. From the simulation result, it is observed that an unwanted glitch is present in the Q node during write '0' operation which is highlighted on the transient result graph.

In this paper, a method is proposed to remove the glitch and reduce the average power dissipation and delay as well. The remaining portion of this paper is arranged in the following manner: Section III contains the explanation of the proposed High Speed Low power 10T SRAM (HS10T). Section IV contains the simulation result for the HS10T cell and the comparison with the LP10T cell. And finally section V concludes the paper.

III. PROPOSED HIGH SPEED LOW POWER 10TSRAM(HS10T)

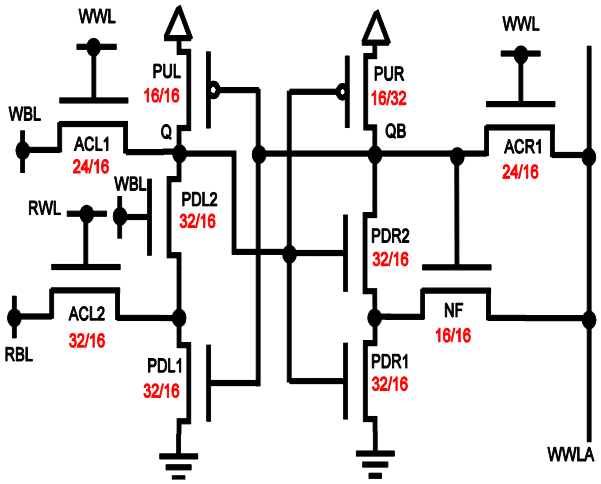

Fig. 4. Proposed High Speed Low Power 10TSRAM(HS10T)

Fig.4 shows the configuration of the proposed High-Speed Low-Power 10TSRAM (HS10T). Transistors ACL1 and ACR1 are pass transistors for write access. The Write Word Line (WWL) control signal is applied to both these transistors. ACL2, controlled by RWL, act as a read-access transistor. A standard inverter with stacked transistor is formed by PUL, PDL2 and PDL1. The Schmitt-Trigger inverter is formed by PUR, PDR2, PDR1 and NF.

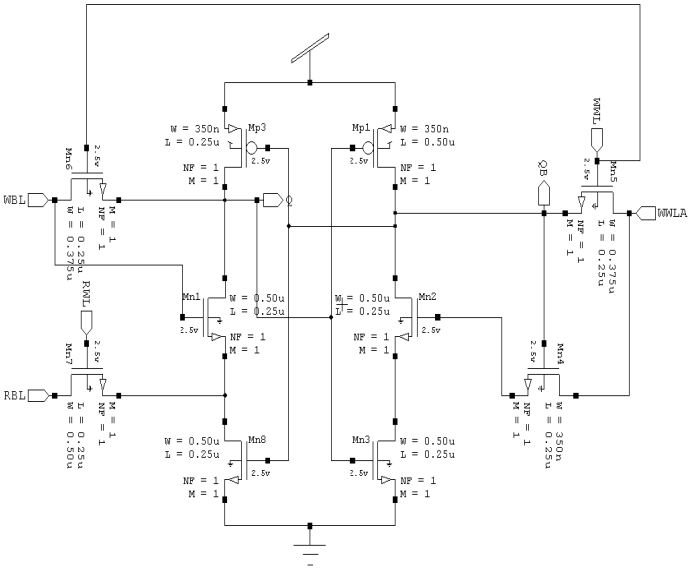

Fig. 5. HS10T cell build in Tanner EDA

In this proposed configuration, the control signal that controls the stacked transistor PDL2 is the Write Bit Line (WBL). The advantages that are obtained by this configuration are the removal of unwanted glitches, decreased propagation delay, and decreased power dissipation. The proposed HS10T cell is simulated in Tanner EDA and verified the operations from the simulation results. HS10T cell build in 250nm technology is shown in Fig. 5. Sizing of the transistors are done to optimize the area, delay and power. Fig. 6. Shows the HS10T simulation result of the transient analysis. The unwanted glitch presented in the LP10T cell is removed by the new proposed configuration. Power and delay measured with the help of T-Spice commands and compared with the LP10T.

IV. VERIFICATION OF OPERATIONS

Control signals for different modes of operations in HS10T are similar to those in the LP10T which are shown in the Table .I. During the hold mode, WWL and RWL are forced to zero, therefore both write access transistors (ACL1 and ACR1) and read access transistor (ACL2) are turned off. This prevents the internal node Q from read and write bit lines.

In the read mode, WWL is forced to zero, therefore the two write access transistors are turned off. All other control signals are forced to become one (high). During read '0' operation, node Q is grounded through PDL2 and PDL1. The High

voltage at the input terminal of the RBL is grounded through PDL1. This transition of RBL from high to low is recognized as zero at the internal node. In the case of read '1' operation, PDL1 is turned off and no path available for the internal node to get connected with ground. And there is no transition at input of the ACL2 ,which is recognized as reading one.

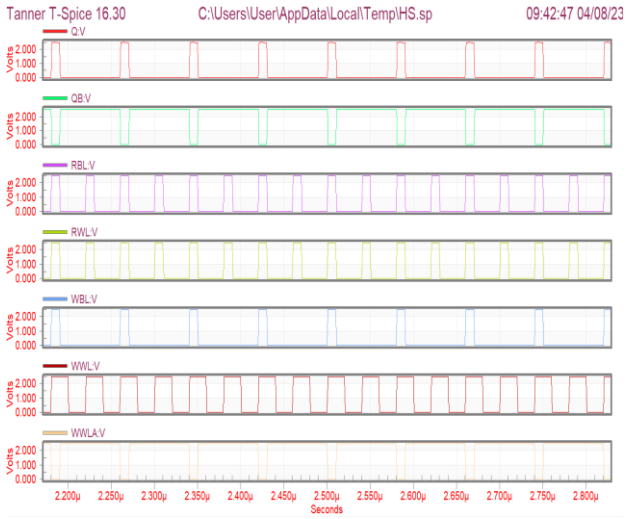

Fig. 6. Simulation result of HS10T

In write operations, RWL control signal is forced to zero, therefore the read bit line (RBL) is decoupled from the internal node. The WWL control signal turns on the write access transistors. For write '0' operation, bit 0(0v) is applied to the write bit line, which is coupled to the node Q through ACL1. Only one path available for node Q to become zero, which is through ACL1. During this operation, PDL2 turned off by WBL and no path created through PDL2 to PDL1, which reduces the series resistance.

For write '1' operation, bit 1(2.5v) is applied to write bit line and coupled to node Q. In this mode, PDL2 is turned on by WBL, therefore it holds the data reliably. Comparison between LP10T and HS10T cells are shown in the TABLE II. Chart in the Fig. 7 Shows the comparison in terms of read delay, write delay and average power dissipation.

TABLE II. COMPARISON BETWEEN LP10T AND HS10T

SRAM cells	LP10T	HS10T
Bit cells Transistors(#)	10	10
Bit lines(#)	2	2
Control signals(#)	3	3
Read delay(ns)	36.3253	33.9816
Write delay(ns)	37.4052	34.8837
Average Power(µw)	2.0704	1.5875

By controlling the ACL2 transistor with WBL in this proposed configuration read delay, write delay and power dissipation can be reduced while maintain read stability and write ability.

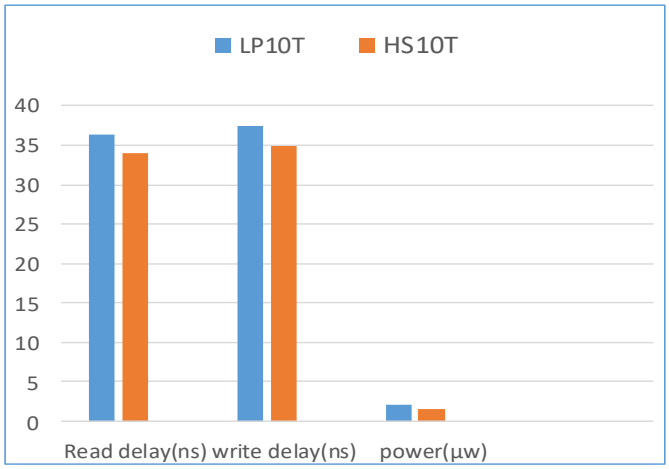

Fig .7 Comparison in terms of delay and power.

V. CONCLUSION

A new HS10T SRAM cell is proposed with improved noise margins. It has good read stability and write ability. The proposed HS10T cell is simulated using the Tanner EDA tool in 250nm technology. Compared to the previous 10T SRAM cell, the proposed model shows more robustness. The speed of the HS10T in terms of read delay and write delay is better than the previous model. The proposed cell consumes less power than the previous model.

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